

# Qucs

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Compact device - circuit macromodel specification

A Curtice level 1 MESFET model

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## Introduction

The Metal and Semiconductor FET (MESFET) is a Schottky-barrier gate FET made from gallium arsenide. It is popular for high frequency applications because of its high electron mobility. The device was developed by Walter R. Curtice<sup>1</sup> in 1980 at the RCA Laboratory in Princeton, New Jersey. USA. The MESFET model presented below is based on a Qucs equation defined device (EDD) which functions as a Curtice level 1 MESFET model with interelectrode capacitances. Basic temperature effects are also included.

## Qucs EDD model for the Curtice MESFET

Parameters

| Name  | Symbol    | Description                                              | Unit               | Default   |
|-------|-----------|----------------------------------------------------------|--------------------|-----------|
| RG    | $R_G$     | external gate resistance                                 | $\Omega$           | 1m        |
| RD    | $R_D$     | external drain resistance                                | $\Omega$           | 1m        |
| RS    | $R_S$     | external source resistance                               | $\Omega$           | 1m        |
| VBR   | $V_{DR}$  | GS breakdown voltage                                     | V                  | $10^{10}$ |
| LG    | $L_G$     | external gate lead inductance                            | H                  | 0         |
| LD    | $L_D$     | external drain lead inductance                           | H                  | 0         |
| LS    | $L_S$     | external source lead inductance                          | H                  | 0         |
| Is    | $I_S$     | diode saturation current                                 | A                  | 10f       |
| N     | $N$       | diode emission coefficient                               |                    | 1         |
| XTI   | $X_{TI}$  | diode saturation current temperature coefficient         |                    | 0         |
| EG    | $E_G$     | diode energy gap                                         | eV                 | 1.11      |
| TAU   | $\tau$    | internal time delay from drain to source                 | s                  | 10p       |
| RIN   | $R_{IN}$  | series resistance to CGS                                 | $\Omega$           | 1m        |
| CGS   | $C_{GS}$  | interelectrode gate-source bias-independent capacitance  | F                  | 300f      |
| CGD   | $C_{GD}$  | interelectrode gate-drain bias-independent capacitance   | F                  | 300f      |
| CDS   | $C_{DS}$  | interelectrode drain-source bias-independent capacitance | F                  | 300f      |
| Tnom  | $T_{NOM}$ | device parameter measurement temperature                 | $^{\circ}\text{C}$ | 27        |
| Temp  | $T$       | device temperature                                       | $^{\circ}\text{C}$ | 27        |
| Alpha | $\alpha$  | coefficient of Vds in tanh function for quadratic model  | 1/V                | 0.8       |

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<sup>1</sup>W.R Curtice, 1980, A MESFET model for use in the design of GaAs integrated circuits, IEEE Transactions on Microwave Theory and Techniques, MTT-28, pp. 448-456.

| Name   | Symbol    | Description                                             | Unit             | Default |
|--------|-----------|---------------------------------------------------------|------------------|---------|
| Beta   | $\beta$   | transconductance parameter                              | A/V <sup>2</sup> | 3m      |
| Lambda | $\lambda$ | channel length modulation parameter for quadratic model | 1/V              | 40m     |
| VTO    | $V_{TO}$  | quadratic model gate threshold voltage                  | V                | -6      |

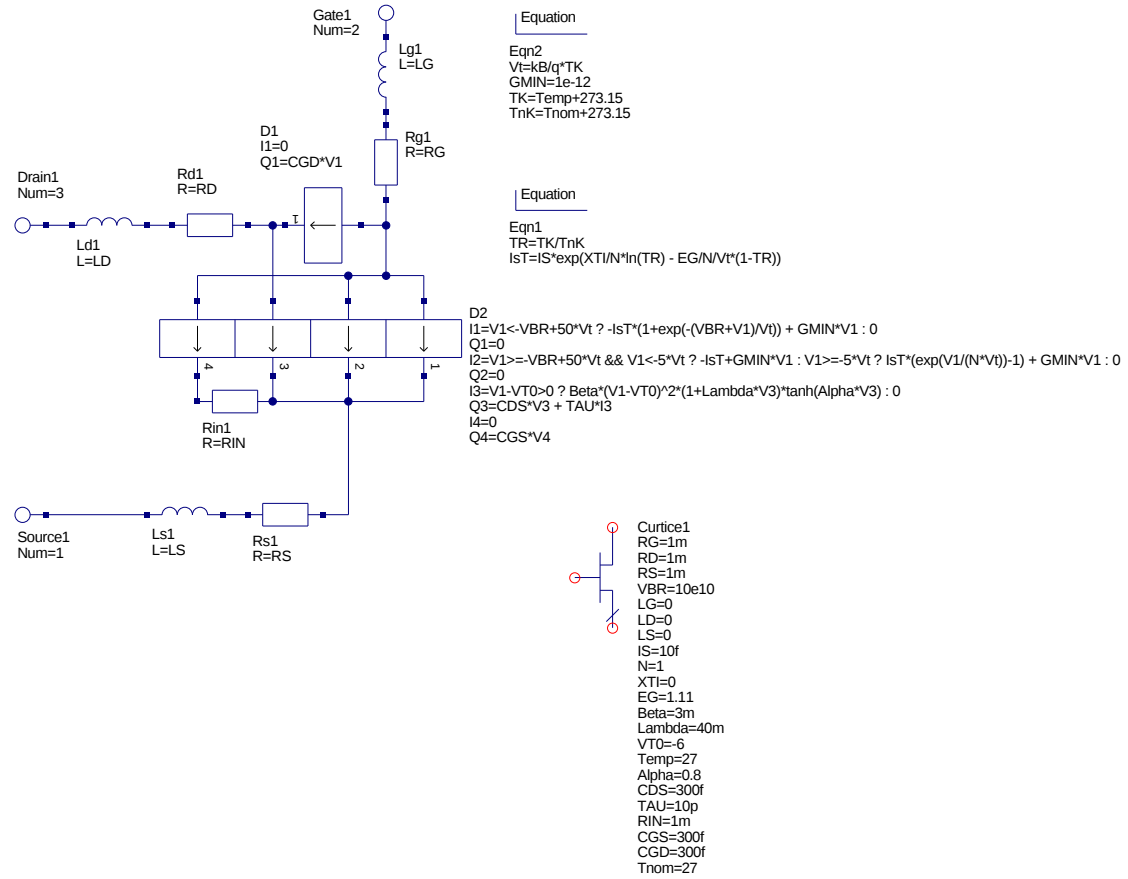


Figure 1: A Qucs EDD model for the Curtice MESFET

## The MESFET equations

- DC characteristics

1. for  $(V_{GS} < -V_{BR} + 50 \cdot V_T)$

$$I_{GS} = -I_S(T) \cdot \left(1 + \exp\left(-\frac{V_{BR} + V_{GS}}{V_T}\right)\right) + G_{MIN} \cdot V_{GS} \quad (1)$$

2. for  $(V_{GS} \geq -V_{BR} + 50 \cdot V_T)$  and  $(V_{GS} < -5 \cdot V_T)$

$$I_{GS} = -I_S(T) + G_{MIN} \cdot V_{GS} \quad (2)$$

3. for  $(V_{GS} \geq -5 \cdot V_T)$

$$I_{GS} = I_S(T) \cdot \left(\exp\left(\frac{V_{GS}}{N \cdot V_T}\right) - 1\right) + G_{MIN} \cdot V_{GS} \quad (3)$$

4. for  $(V_{GS} - V_{TO}) > 0$

$$I_{DS} = \beta \cdot (V_{GS} - V_{TO})^2 \cdot (1 + \lambda \cdot V_{DS}) \cdot \tanh(\alpha \cdot V_{DS}) \quad (4)$$

Where

$$I_S(T) = I_S \cdot \exp\left(\frac{X_{TI}}{N} \cdot \ln(TR) - (E_G/N/V_T) \cdot (1 - TR)\right) \quad (5)$$

$$Tr = \frac{TK}{TnK} \quad \text{and} \quad TK = T + 273.15, \quad TnK = T_{NOM} + 273.15 \quad (6)$$

- MESFET charge equations

- 1.

$$Q_{GS} = C_{GS} \cdot V_{GS} \quad (7)$$

- 2.

$$Q_{GD} = C_{GD} \cdot V_{GD} \quad (8)$$

- 3.

$$Q_{DS} = C_{DS} \cdot V_{DS} + \tau \cdot I_{DS} \quad (9)$$

# Test circuits and simulation results

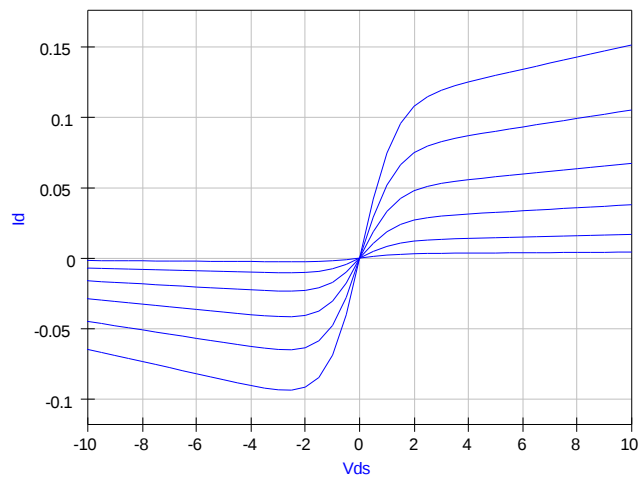
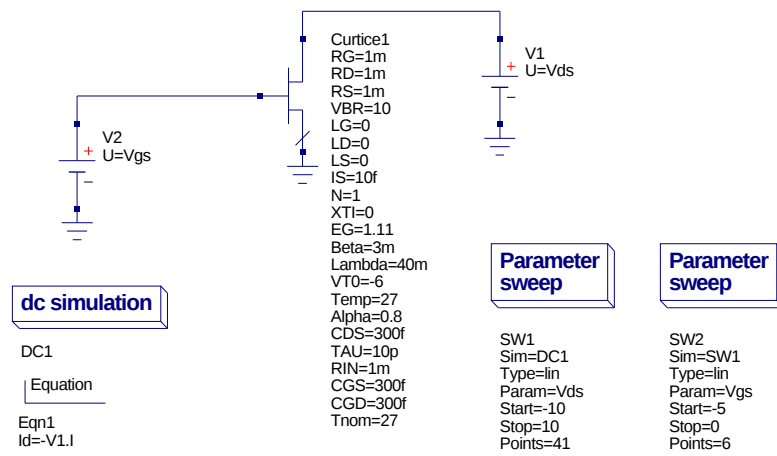


Figure 2: DC test circuit and  $I_d$ - $V_{ds}$  characteristics

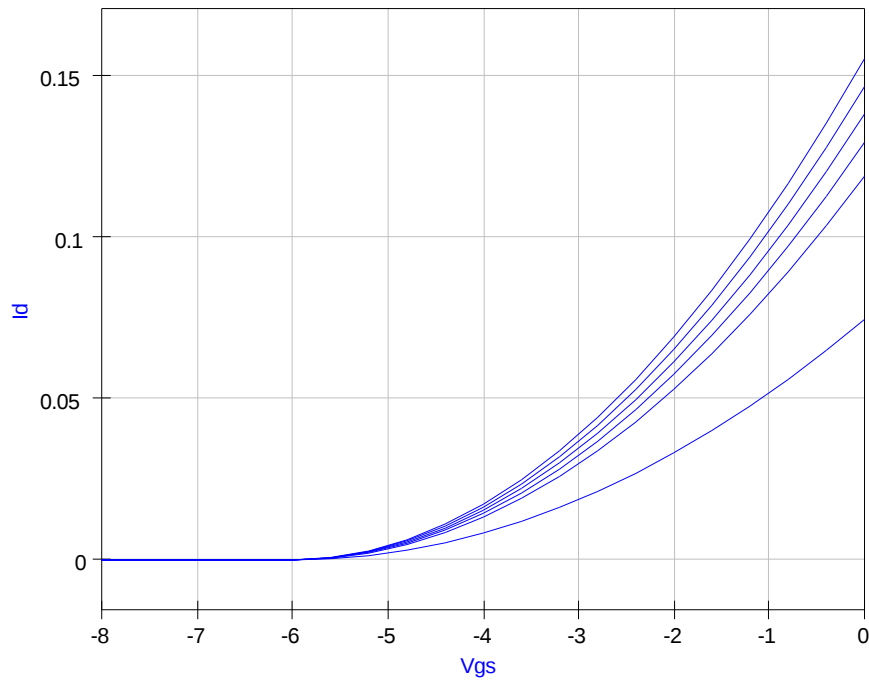
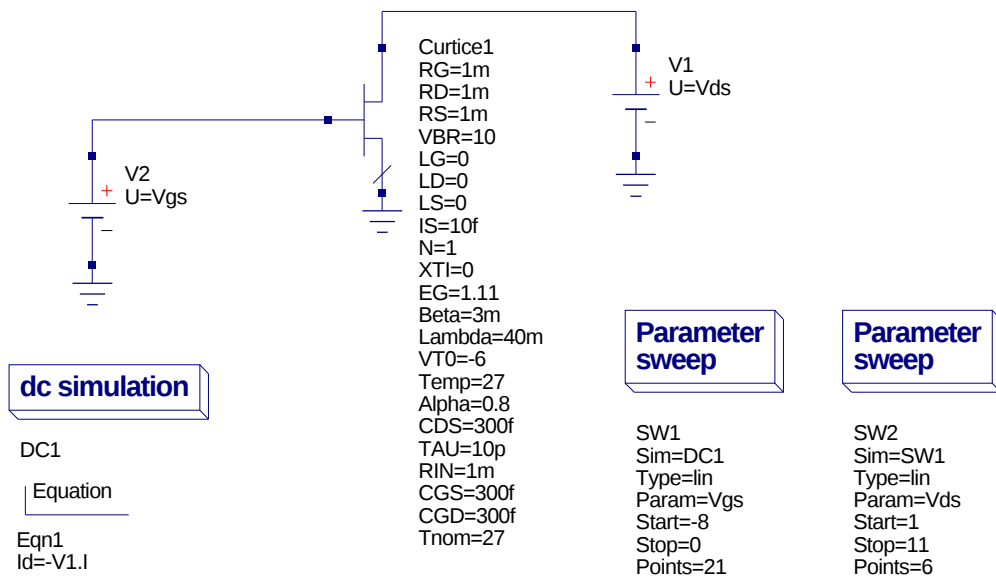


Figure 3: DC test circuit and  $I_d$ - $V_{gs}$  characteristics

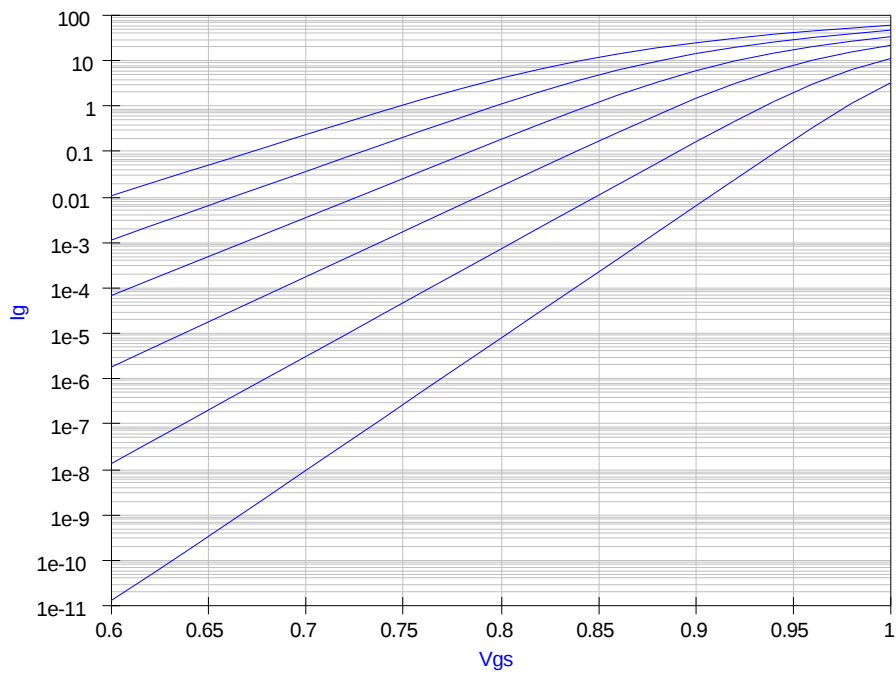
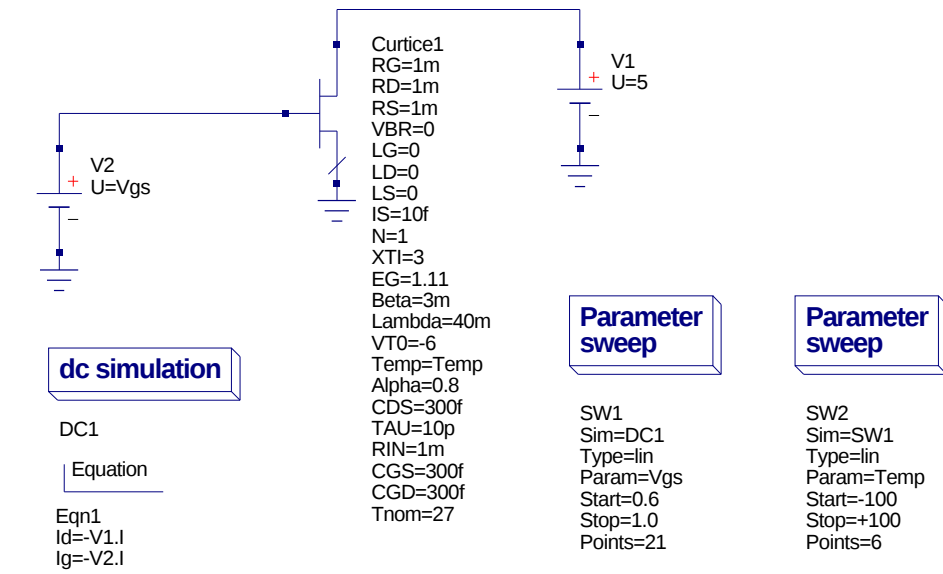


Figure 4: DC test circuit and  $I_g$ - $V_{gs}$  characteristics

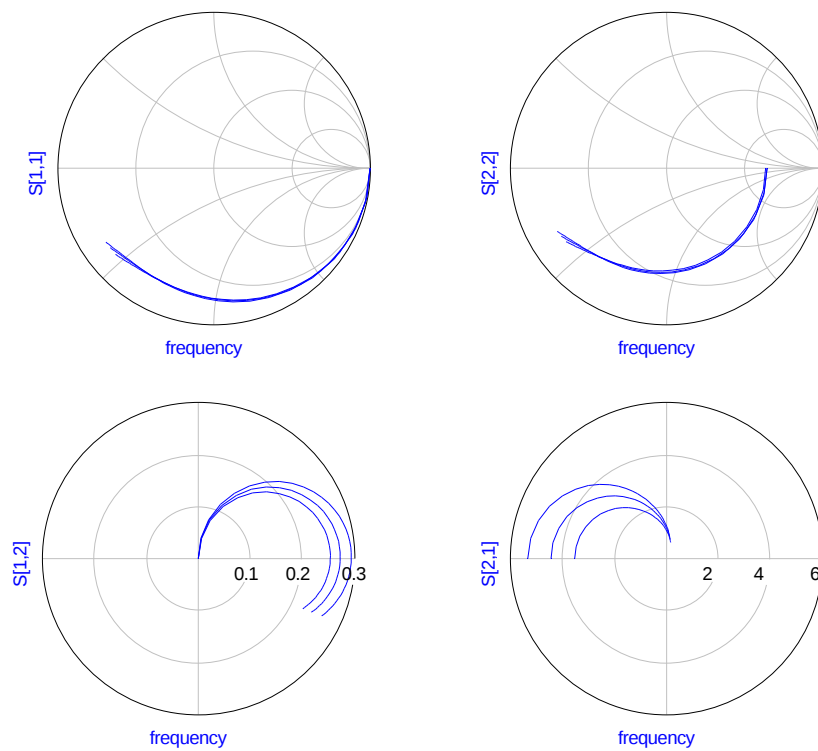
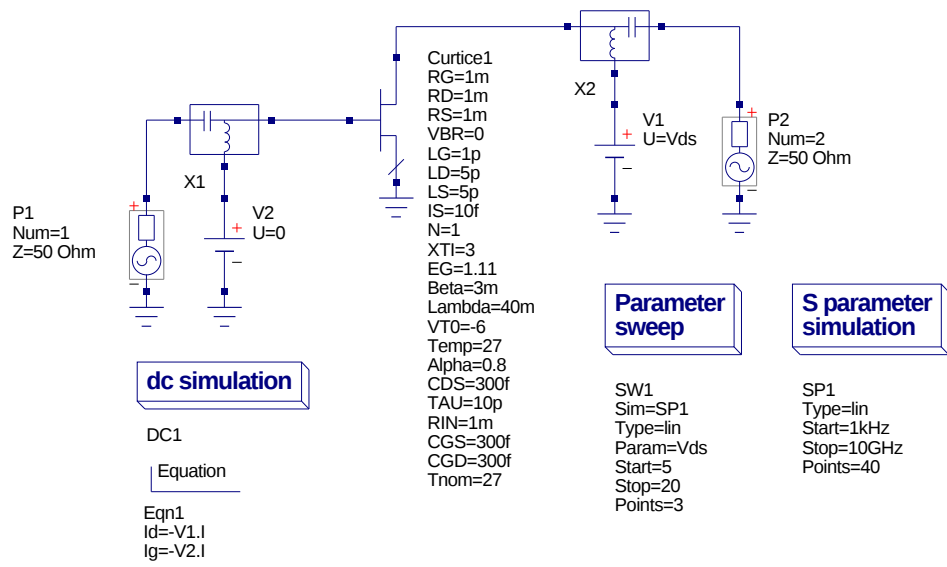


Figure 5: S parameter test circuit and characteristics